

REMARKS

Claims 8-10 and 12-22 are pending. Claims 8, 9 and 10 has been amended. Claims 1-7 and 11 have been canceled. Claims 13-22 have been added. Applicant requests reconsideration and reexamination of the pending claims.

Rejections under 35 U.S.C. 112, second paragraph:

Claims 1-12 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite.

Claims 8 and 9 are now written in independent form and include the features of Claim 1. Thus, Claims 8 and 9 have been amended to include the relative difference in the thickness claimed therein. Claim 10 has been amended to include the relative difference in the thickness claimed therein. Accordingly, Claims 8, 9 and 10 and the claims, which depend therefrom, are now in condition for allowance.

Rejection under 35 U.S.C. 102(e):

Claims 1-7, and 10-12 were rejected under 35 U.S.C. 102(e) as being anticipated by Gardner et al., U.S. Patent No. 6,097,062. Applicant overcomes the rejection as follows.

Claim 10 has been amended to set forth “etching said first portion of said gate insulating layer over said third region to form a second portion....” The etching of the gate insulating layer over the third region creates the “second portion having a second thickness” less than the first thickness. Applicant could find no teaching or suggestion of etching a portion of a gate insulating layer to form a gate insulating layer with variable thickness.

In contrast, Gardner et al. discloses the formation of a gate dielectric 122 with variable thickness created as a result of “substantial lack of nitrogen impurities within the proximal portions 114.... The relatively higher oxidation rate results in a thicker dielectric film above the proximal portions 114 relative to the portions of gate dielectric 122 over distal portions 115 of substrate 102.” (Gardner et al., col. 5, lines 15-22) Applicant could find no teaching or suggestion of etching as set forth in Claim 10. Accordingly Claim 10 is allowable over the cited reference.

Claim 12 depends from Claim 10 and is therefore allowable for at least the same reasons as Claim 10.

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Rejection under 35 U.S.C. 103(a):

Claims 1-12 were further rejected under 35 U.S.C. 103(a) as being unpatentable over Gardner et al., and further in view of applicant's admitted prior art. Applicant overcomes the rejection as follows.

Claims 8 and 9 have been amended to independent form. Applicant submits that as to Claims 8 and 9 Gardner et al. should be disqualified as a reference under 35 U.S.C. 103(c).

As set forth in MPEP 706.02(l)(3) the reference may be disqualified for the following reasons: (1) The Gardner et al. reference and the present application were, at the time the invention was made, owned by, or subject to an obligation of assignment to Advanced Micro Devices, Inc. of Sunnyvale, CA; (2) the present application has an effective filing date after November 29, 1999 and the reference qualifies as a 35 U.S.C. 102(e) reference; and (3) the reference is used in a rejection under 35 U.S.C. 103(a).

Applicant respectfully disagrees with the Examiner that Claims 8 and 9 are suggested or taught in the disclosure of Gardner et al. However, since Gardner et al. should be disqualified as a reference, Applicant sees no need to comment on the substantive rejection to Claims 8 and 9 at this time. Accordingly, Claims 8 and 9 are allowable over the cited reference in view of Applicant's disclosure.

New Claims

Claims 13-22 have been added with no new matter being added thereby. Claims 13-22 were previously claims that depended from Claim 1 as originally filed and therefore have been examined.

Dependent Claims

Claims 13-17 depend from Claim 8 and are therefore allowable for at least the same reasons as Claim 8. Claims 18-22 depend from Claim 9 and are therefore allowable for at least the same reasons as Claim 9.

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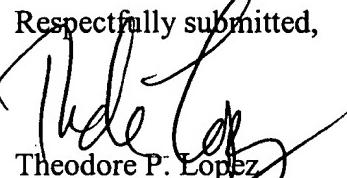
CONCLUSION

For the above reasons, pending Claims 8-10 and 12-22 are now in condition for allowance and allowance of the application is hereby solicited. If the Examiner has any questions or concerns, the Examiner is hereby requested to telephone Applicant's Attorney at (949) 718-5200.

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Respectfully submitted,


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ATTACHMENT A

Please cancel Claims 1-7.

8. (Amended) [A memory cell as in claim 1, further comprising]

A memory cell comprising:

a semiconductor substrate having a first region and a second region of one conduction type and a third region therebetween of an opposite conduction type;

a gate insulating layer formed over said substrate, the gate insulating layer having a first thickness formed over said first region and said second region, and a second thickness formed over said third region, said first thickness being greater than said second thickness;
and

a control gate formed on said gate insulating layer.

9. (Amended) [A memory cell as in claim 1, further comprising]

A memory cell comprising:

a semiconductor substrate having a first region and a second region of one conduction type and a third region therebetween of an opposite conduction type; and

a gate insulating layer formed over said substrate, the gate insulating layer having a first thickness formed over said first region and said second region, and a second thickness formed over said third region, said first thickness being greater than said second thickness;
and

an ONO stack formed on said gate insulating layer.

10. (Amended) A method for fabricating a memory cell, the method comprising:

providing a semiconductor substrate having a first region and a second region of one conduction type and a third region therebetween of an opposite conduction type;

forming a first portion of a gate insulating layer over said first region and said second region; and

etching said first portion [forming a second portion] of said gate insulating layer over said third region to form a second portion,

said first portion having a first thickness said second portion having a second thickness, said first thickness being greater than said second thickness.

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